

WHAT IS CLAIMED IS:

1. A sales method for selling semiconductor devices by way of a communication network, said method comprising:

5 presenting function-related information and price-
related information on partially good semiconductor
devices having one or more than one unusable functions
to the client terminals by way of the communication
network and prompting the client terminals to provide
10 purchase/non-purchase information; and

determining the possibility of successful transactions on the basis of the purchase/non-purchase information provided from client terminals.

2. A sales method for selling semiconductor
15 devices by way of a communication network, said method
comprising:

presenting function-related information on a semiconductor device to be possibly purchased by way of the communication network; and

20 providing purchase/non-purchase information on the
basis of the function-related information and the
price-related information on partially good semicon-
ductor devices having one or more than one unusable
functions and the function specified in said
25 function-related information provided by way of the
communication network.

3. The sales method according to claim 1, wherein

the price-related information on each of the partially good products is defined on the basis of the trend of the price zone of the market for similar partially good products obtained by referring to the function-related information of the partially good product.

4. The sales method according to claim 2, wherein the price-related information on each of the partially good products is defined on the basis of the trend of the price zone of the market for similar partially good products obtained by referring to the function-related information of the partially good product.

5. The sales method according to claim 1, wherein the lower limit of the price of each of the partially good products is set at a level not lower than the cost of disposing the partially good product as waste.

6. The sales method according to claim 2, wherein the lower limit of the price of each of the partially good products is set at a level not lower than the cost of disposing the partially good product as waste.

7. The sales method according to claim 2, wherein each of said partially good products comprises:
a plurality of cell arrays;
a selection control circuit for generating and

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an array selection circuit for generating said
5 internal address signals on the basis of an external
address signal and said selection control signal and
outputting it to said plurality of cell arrays; wherein

15 8. A sales system for selling semiconductor
devices by way of a communication network, said system
comprising:

a partially good products presenting means for presenting function-related information and price-related information on partially good semiconductor devices having one or more than one unusable functions and the functions specified in the function-related information obtained by said products to be possibly

purchased registering means and prompting the client terminals to provide purchase/non-purchase information; and

5 a possibility of successful transaction
determining means for obtaining purchase/non-purchase
information on said partially good products from the
client terminals and determining the possibility of
successful transactions on the basis of the purchase/
non-purchase information provided from client
10 terminals.

9. The sales system according to claim 8, wherein
the price-related information on each of the
partially good products is defined on the basis of the
trend of the price zone of the market for similar
15 partially good products obtained by referring to the
function-related information of the partially good
product.

10. The sales system according to claim 8, wherein
the lower limit of the price of each of the
20 partially good products is set at a level not lower
than the cost of disposing the partially good product
as waste.

11. The sales system according to claim 8, wherein
each of said partially good products comprises:
25 a plurality of cell arrays;
a selection control circuit for generating and
outputting a selection control signal to be used for

generating internal address signals for selecting at least one of said plurality of cell arrays;

an array selection circuit for generating said internal address signal on the basis of an external address signal and said selection control signal and outputting it to said plurality of cell arrays;

said array selection circuit being adapted to define the correspondence of each piece of information contained in said selection control signal and a selectable combination of any of said plurality of cell arrays and output internal address signals for selecting any of the combinations of said plurality of cell arrays.

12. A sales program product for causing a computer system to sell semiconductor devices by way of a communication network, said product comprising:

a recording medium;

a first means stored in said recording medium and adapted to issue a command to said computer system for obtaining function-related information on the semiconductor devices possibly to buy from the client terminals by way of a communication network;

a second means stored in said recording medium and adapted to display function-related information and price-related information on the partially good semiconductor devices having the functions shown in said function-related information and also unusable

5 a third means stored in said recording medium and
adapted to obtain purchase/non-purchase information on
each of said partially good products from said client
terminals and determining purchase/non-purchase of the
product on the basis of said purchase/non-purchase
0 information.

a plurality of cell arrays;
a selection control circuit for generating and
outputting a selection control signal to be used for
generating internal address signals for selecting at
least one of said plurality of cell arrays; and

an array selection circuit for generating said internal address signals on the basis of an external address signal and said selection control signal and outputting it to said plurality of cell arrays; wherein said array selection circuit being adapted to define the correspondence of each piece of information contained in said selection control signal and a selectable combination of any of said plurality of cell arrays and output internal address signals for selecting any of the combinations of said plurality of cell arrays.

14. The semiconductor device according to claim 13, wherein

said selection control signal specifies whether the information indicated by said selection control signal is reflected to said internal address signals or not; and

said array selection circuit generates and outputs internal address signals for selecting said plurality of cell arrays on the basis of said external address signal if the information indicated by said selection control signal is not reflected to said internal address signals.

15. The semiconductor device according to claim 14, wherein

said internal address signal is not modified by the information indicated by said external address signal if the information indicated by said selection control signal is reflected to said internal address signals.

16. The semiconductor device according to claim 13, wherein

said array selection circuit outputs information for specifying said semiconductor device and a mode signal for modifying the functions of said semiconductor device according to said external address signal and said selection control signal.

17. The semiconductor device according to

claim 13, further comprising:

at least one pad; and wherein

said selection control signal being defined by
a combination of binary signals, each representing
existence or absence of a state of being bonded of
a corresponding one of said pads.

18. The semiconductor device according to
claim 13, further comprising:

at least one fuse; and wherein

said selection control signal being defined by
a combination of binary signals, each representing
existence or absence of an electrically or physically
broken state of a corresponding one of said fuses.

19. The semiconductor device according to
claim 13, further comprising:

at least one register circuit; and wherein

said selection control signal being defined by
a combination of binary signals, each being written in
the corresponding one of said register circuits.

20. The semiconductor device according to
claim 13, further comprising:

a preliminary control signal generation circuit
for outputting a plurality of preliminary control
signals to said selection control circuit; and wherein

said selection control circuit being adapted to
select one of said plurality of preliminary control
signal from said preliminary control signal generation

21. The semiconductor device according to
claim 13, wherein

5 said internal address signals provide at least
three combinations for selecting any of said plurality
of memory cell arrays.

10 said array selection circuit is connected to
function modifiable circuits whose functions can be
modified according to said mode signal and said
function modifiable circuits are modified for the
functions according to the input of said mode signal
15 from said array selection circuit.

said array selection circuit is connected to
an information holding circuit adapted to store
20 information on the semiconductor device and rewrite the
information on the semiconductor device according to
the input of said mode signal from said array selection
circuit.

each of said plurality of memory cell arrays is provided with a parity cell array;

said mode signal is applied to a parity bit input/output circuit; and

the operation of said parity bit input/output circuit being suspended according to the input of said mode signal.

25. The semiconductor device according to claim 13, wherein

each of said plurality of memory cell arrays is provided with a parity cell array;

said address selection signal being connected to a parity bit input/output circuit and a chip information circuit; and

said internal address signals and said mod signal satisfy the requirements listed below;

the mode signal is output to indicate rewriting of the address space to said chip information circuit when said internal address signals suspends the functions of any of said memory cell arrays; and

a signal for suspending the functions of said parity bit input/output circuit is output to said parity bit input/output circuit and the mode signal for rewriting the address space is output to said chip information circuit when said internal address signals suspends the functions of any of said memory cell arrays.

26. A semiconductor device comprising:

a selection control circuit for generating and

outputting a control signal to be used for generating
a mode signal; and

5 a mode signal generation circuit for generating
and outputting said mode signal according to an
external address and said control signal; wherein

said mode signal being adapted to modify the
information specifying said semiconductor device and
the functions of the semiconductor device.

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